AF/2811/#
RFW

Docket No.: SON-2010
(80001-2010)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hisao Hayashi et al.

Application No.: 09/772,986 Confirmation No.: 2637

Filed: January 31, 2001 Art Unit: 2811

For: THIN FILM SEMICONDUCTOR DEVICE, DISPLAY DEVICE USING SUCH THIN FILM SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF Examiner: T. F. Tran

TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Three copies of an Appellant's Supplemental Brief on Appeal for the above-referenced application are being filed herewith. Thus, consideration of the Appeal Brief is respectfully requested.

An Appeal Brief and fee was filed on December 31, 2003. Thus, it is believed that **no fees are due**. M.P.E.P. §1208.02. However, if a fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013.

Dated: July 7, 2004

Respectfully submitted,

By _____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant

Docket No.: SON-2010
(80001-2010)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hisao Hayashi et al.

Application No.: 09/772,986 Confirmation No.: 2637

Filed: January 31, 2001 Art Unit: 2811

For: THIN FILM SEMICONDUCTOR DEVICE, DISPLAY DEVICE USING SUCH THIN FILM SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF Examiner: T. F. Tran

SUPPLEMENTAL APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Supplemental Appeal Brief, submitted under 37 C.F.R. §§ 1.192 and 1.193(b)(2)(ii), requesting reinstatement of the Appeal in response to the non-final rejection of the Examiner dated March 12, 2004 (hereinafter the "Office Action") reopening prosecution of this case.

The Notice of Appeal was filed on November 25, 2003 and the fee for an Appeal Brief was filed on December 31, 2003.

Submitted herewith are two additional copies of this Appeal Brief. Applicants (hereinafter "Appellants"), respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the present patent application referenced above.

Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

This brief contains items under the following headings as required by 37 C.F.R. §1.192 and M.P.E.P. §1206:

I. REAL PARTY IN INTEREST

The Real "Party-In-Interest" of the present application is Sony Corporation of Tokyo, Japan ("Sony") located at 7-35 Kitashinagawa 6-Chome, Shinagawa-Ku, Tokyo, Japan. An assignment of all rights in the present application to Sony was recorded with the U.S. Patent and Trademark Office on January 31, 2001 at **Reel 011519, Frame 0913**.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 12 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 9-12.

2. Claims withdrawn from consideration but not canceled: none.

3. Claims pending: 1-8 and 13-16.

4. Claims allowed: none.

5. Claims rejected: 1-8 and 13-16.

C. Claims On Appeal

The claims on appeal are claims 1-8 and 13-16.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the rejection. A copy of all claims on appeal is attached hereto as an Appendix.

V. SUMMARY OF INVENTION

By way of background, the present invention relates to a thin film semiconductor device for use as a display. Page 1, lines 6-7. The thin film semiconductor device is formed as an integrated circuit on an insulating substrate with bottom gate structured thin film transistors. Page 6, lines 6-10. The gate electrodes of the semiconductor device are positioned at the bottom-most portion of the structure, with the gate insulating film disposed thereover. Page 6, lines 10-12. A semiconductor thin film is then stacked on top of the gate insulating film. The gate electrode is comprised of a metallic material that has a thickness of less than 100nm. Page 6, lines 12-15. Referring to the specification at page 7, lines 24-31, making the thickness of the gate electrode less than 100 nm reduces the thermal capacity of the gate electrode. Additionally, the gate insulating film covering the gate electrodes is comprised of a film, whose thickness is greater than the thickness of the gate electrodes. Page 9, lines 28-30. Making the thickness of

the gate electrode less than 100nm reduces the thermal capacity of the gate electrode, which results in a similar thermal condition between the gate electrode and insulating substrate. Page 9, line 31-page 10, line 3. This enlarges the process margin resulting from the laser anneal treatment used during the manufacturing process. Page 10, lines 3-5. Making the thickness of the gate insulating film greater than the thickness of the gate electrode ensures that the benefits of reducing the thickness of the gate electrode below 100 nm are not offset. Page 9, line 28-page 10, line 14. However, if the thickness of the gate insulating film located between the gate electrodes in a semiconductor thin film is too thin, the effect of reducing the thickness of the gate electrode is offset. Page 10, lines 5-7. Accordingly, the thickness of the gate insulating film is designed greater than the thickness of the gate electrodes. Page 10, lines 7-9.

VI. ISSUES

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 1-8, 13 and 15 under 35 U.S.C. §102 as allegedly being anticipated by Japanese Publication No. 10-209467 to Hisao et al (Hisao).

Whether the Examiner erred in rejecting claims 14 and 16 under 35 U.S.C. §103 as allegedly being obvious over Hisao.

This issue will be discussed hereinbelow.

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Claims 1, 3 and 13 stand or fall together.

Claim 2 stands or falls separately.

Claim 4 stands or falls separately.

Claims 5, 7 and 15 stand or fall together.

Claim 6 stands or falls separately.

Claim 8 stands or falls separately.

Claim 14 stands or falls separately.

Claim 16 stands or falls separately.

The arguments set forth in the following section provide reasons why these groups are considered patentable, 37 C.F.R. 1.192 (c)(7).

VIII. ARGUMENTS

In the non-final Office Action of March 12, 2004:

The Examiner rejected claims 1-8, 13 and 15 under 35 U.S.C. §102 as allegedly being anticipated by Hisao.

The Examiner rejected claims 14 and 16 under 35 U.S.C. §103 as allegedly being obvious over Hisao.

For at least the following reasons, Appellant submits that this rejection is both technically and legally unsound and should therefore be reversed.

General Matters

M.P.E.P. 707.07(f) states that "the importance of answering such arguments is illustrated by In re Herrmann, 261 F.2d 598, 120 USPQ 182 (CCPA 1958) where the applicant urged that the subject matter claimed produced new and useful results. The court noted that since applicant's statement of advantages was not questioned by the examiner or the Board of Appeals, it was constrained to accept the statement at face value and therefore found certain claims to be allowable. See also In re Soni, 54 F.3d 746, 751, 34 USPQ2d 1684, 1688 (Fed Cir. 1995) (Office failed to rebut applicant's argument)."

The Examiner erred in rejecting claims 1-8, 13 and 15 under 35 U.S.C. §102 as allegedly being anticipated by Hisao.

Anticipation

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 1, 3, 13

This rejection is respectfully traversed at least for the following reasons.

Claim 1 and the claims dependent thereon are drawn to a thin film semiconductor device comprising:

an insulating substrate; and

a thin film transistor formed on said insulating substrate, wherein

said thin film transistor is formed in a bottom gate structure having gate electrode, a gate insulating film, and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

Hisao arguably teaches a thin film semiconductor device having a gate electrode 5 having an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (figure 2(A), paragraph [0012]).

However, claim 1 provides that the gate electrode is made of metallic material having a thickness of *less than 100 nm*. Although the Office Action contends that gate electrode 5 of Hisao allows for a thickness being *slightly less than 100 nm* (Office Action at page 3), the Office Action fails to highlight any teachings within Hisao or other evidence in support of this contention. As a result, the contention made within the Office Action that gate electrode 5 of Hisao allows for a thickness being *slightly less than 100 nm* is conclusory at best. See *Mark I Marketing Corp. v. R.R. Donnelley & Sons Co.*, 36 USPQ2d 1095, 1098-99 (Fed. Cir. 1995). Thus, the Office Action fails to show that Hisao teaches a gate electrode made of metallic material having a thickness of less than 100 nm.

Additionally within claim 1, the gate insulating film has a thickness that is greater than the thickness of the gate electrode. In this regard, Hisao arguably teaches an insulator layer 4 having a thickness of 100-200 nm (figure 2(C), paragraph [0016]). But because Hisao arguably teaches a thin film semiconductor device having a gate electrode 5 with an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (figure 1, paragraph [0012]), the Office Action fails to show that the gate insulating film 4 of Hisao has a thickness that is greater than the thickness of the gate electrode 5 of Hisao.

Thus, each and every element as set forth in the claim is not found, either expressly or inherently described, within Hisao.

Claim 2

In addition to the reasons provided herein within respect to claim 1, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 2, said gate insulating film has a thickness thicker than the thickness of said gate electrode.

However, Hisao arguably teaches an insulator layer 4 having a thickness of 100-200 nm (figure 2(C), paragraph [0016]) and arguably teaches a thin film semiconductor device having a gate electrode 5 having an upper layer 5a of 50-200 nm and a lower layer 5b of 50-200 nm (figure 1, paragraph [0012]). As a result, the Office Action fails to show that the gate

insulating film 4 of Hisao has a thickness that is greater than the thickness of the gate electrode 5 of Hisao.

Claim 4

In addition to the reasons provided herein within respect to claim 1, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 4, said gate electrode has a multi-layered structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

Hisao arguably teaches an upper layer 5a of a ITO film, TiN film, and TiON film, or Nichrome (paragraph [0012]) and teaches a lower layer 5b of W, Cr, Mo, and Ti, (paragraph [0012]).

However, the Office Action fails to show that the upper layer 5a of Hisao has comparatively low heat conductivity and high electric resistance, and that the lower layer 5b of Hisao has comparatively high heat conductivity and low electric resistance.

Claims 5, 7, 15

This rejection is respectfully traversed at least for the following reasons.

Claim 5 and the claims dependent thereon are drawn to a display device comprising:

an insulating substrate;

pixels arranged in a matrix form; and

thin film transistors for driving said respective pixels, wherein said pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode, a gate insulating film and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100 nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

Hisao arguably teaches a thin film semiconductor device having a gate electrode 5 having an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (figure 2(A), paragraph [0012]).

However, claim 5 provides that the gate electrode is made of metallic material having a thickness of *less than 100 nm*. Although the Office Action contends that gate electrode 5 of Hisao allows for a thickness being *slightly less than 100 nm* (Office Action at page 3), the Office Action fails to highlight any teachings within Hisao or other evidence in support of this contention. As a result, the contention made within the Office Action that gate electrode 5 of Hisao allows for a thickness being *slightly less than 100 nm* is conclusory at best. See *Mark I Marketing Corp. v. R.R. Donnelley & Sons Co.*, 36 USPQ2d 1095, 1098-99 (Fed. Cir. 1995). Thus, the Office Action fails to show that Hisao teaches a gate electrode made of metallic material having a thickness of less than 100 nm.

Additionally within claim 5, the gate insulating film has a thickness that is greater than the thickness of the gate electrode. In this regard, Hisao arguably teaches an insulator layer 4 having a thickness of 100-200 nm (figure 2(C), paragraph [0016]). But because Hisao arguably teaches a thin film semiconductor device having a gate electrode 5 with an upper layer 5a of about 50-300 nm and a lower layer 5b of 50-200 nm (figure 1, paragraph [0012]), the Office Action fails to show that the gate insulating film 4 of Hisao has a thickness that is greater than the thickness of the gate electrode 5 of Hisao.

Thus, each and every element as set forth in the claim is not found, either expressly or inherently described, within Hisao.

Claim 6

In addition to the reasons provided herein within respect to claim 5, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 6, said gate insulating film has a thickness thicker than the thickness of said gate electrode.

However, Hisao arguably teaches an insulator layer 4 having a thickness of 100-200 nm (figure 2(C), paragraph [0016]) and arguably teaches a thin film semiconductor device having a gate electrode 5 having an upper layer 5a of 50-200 nm and a lower layer 5b of 50-200 nm (figure 1, paragraph [0012]). As a result, the Office Action fails to show that the gate insulating film 4 of Hisao has a thickness that is greater than the thickness of the gate electrode 5 of Hisao.

Claim 8

In addition to the reasons provided herein within respect to claim 5, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 8, said gate electrode has a multi-layered structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

Hisao arguably teaches an upper layer 5a of a ITO film, TiN film, and TiON film, or Nichrome (paragraph [0012]) and teaches a lower layer 5b of W, Cr, Mo, and Ti, (paragraph [0012]).

However, the Office Action fails to show that the upper layer 5a of Hisao has comparatively low heat conductivity and high electric resistance, and that the lower layer 5b of Hisao has comparatively high heat conductivity and low electric resistance.

The Examiner erred in rejecting claims 14 and 16 under 35 U.S.C. §103 as allegedly being obvious over Hisao.

Obviousness

"The Patent and Trademark Office (PTO) has the burden of showing a prima facie case of obviousness." *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). "In determining the propriety of the Patent Office case for prima facie obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification." *In re Taborsky*, 183 USPQ 50, 55 (CCPA 1974). Moreover, *prima facie* obviousness of a claimed invention is established "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Claim 14

In addition to the reasons provided herein within respect to claims 1 and 13, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 14, the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

The Office Action admits that the gate electrode being 90 nm is not found within Hisao. Yet the Office Action contends, ***without providing any evidentiary support,*** that a gate electrode of 90 nm would have been obvious nonetheless.

In response to this contention, this unsupported assertion amounts to nothing more than conclusions that are personal in nature. The teachings, suggestions or incentives supporting the obviousness-type rejection must be clear and particular. Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

The Office Action relies upon hindsight for the features missing within Hisao. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention,

using the applicant's structure as a template and selecting elements from references to fill the gaps. The references themselves must provide some teaching whereby the applicant's combination would have been obvious" (citations omitted). *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). See also *In re Dembiczak*, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999)(rejection based upon hindsight is reversed).

As a rule, "assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

In addition, this assertion amounts to nothing more than an "obvious-to-try" situation. Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990). Moreover, "an invention is 'obvious to try' where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful." *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, the Office Action fails to set forth a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious to try" is not the standard under §103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

Alternatively, another way for a patent applicant to rebut a *prima facie* case of obviousness is to make a showing of "unexpected results," i.e., to show that the claimed invention exhibits some superior property or advantage that a person of ordinary skill in the relevant art would have found surprising or unexpected. *In re Geisler*, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997).

"All evidence of nonobviousness must be considered when assessing patentability." *Richardson-Vicks Inc. v. The Upjohn Co.*, 44 USPQ2d 1181, 1186 (Fed. Cir. 1997).

"Consistent with the rule that all evidence of nonobviousness must be considered when assessing patentability, the PTO must consider comparative data in the specification in determining whether the claimed invention provides unexpected results." *In re Soni*, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995). See also, *In re Wright*, 6 USPQ2d 1959, 1962 (Fed. Cir. 1988).

In this regard figure 3 of the above-identified application is a graph showing the relation between a film thickness of gate electrodes and a process margin, whereas figure 4 of the above-identified application is a graph showing the relation between a film thickness of the gate electrodes and a quantity of pinholes.

"When an applicant seeks to overcome a prima facie case of obviousness by showing improved performance in a range that is within or overlaps with a range disclosed in the prior art, the applicant must 'show that the [claimed] range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.'" *In re Geisler*, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997).

By making the thickness of the gate electrodes 5 to be less than 100 nm, thermal capacity can be reduced and the difference in thermal condition on the gate electrodes 5 and the insulating substrate 1 is made small, thereby trying to enlarge a process margin occurred by the laser anneal treatment (specification at page 9, line 31 to page 10, line 4). It is also clear from the graph of figure 3 that the film thickness of the gate electrodes is required to be set to less than 100 nm (specification at page 12, lines 14-15). Moreover, figure 4 shows that by making the thickness of the gate electrodes to be less than 100 nm, emergence of the pinholes may almost completely be prevented (specification at page 12, lines 22-23).

If the thickness of the gate insulating film 4 located between the gate electrodes 5 and the semiconductor thin film 2 is too thin, an effect of reducing the thickness of the gate electrodes 5 is offset (specification at page 10, lines 4-7). Therefore, the thickness of the gate insulating film 4 is made to become greater than the thickness of the gate electrodes 5 (specification at page 10, lines 7-9). For instance, when the thickness of the gate electrodes 5 is

90 nm, the thickness of the gate insulating film is made to be 110 nm (specification at page 10, lines 9-11).

"An applicant relying on comparative tests to rebut a prima facie case of obviousness must compare his claimed invention to the closest prior art." *In re De Blauwe*, 222 USPQ 191, 196 (Fed. Cir. 1984).

The Office Action provides Hisao as the closest cited prior art. Yet, the Office Action admits that the gate electrode being 90 nm is not found within Hisao.

Claim 16

In addition to the reasons provided herein within respect to claims 5 and 15, the rejection of this claim is respectfully traversed at least for the following reason.

Within claim 16, the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

The Office Action admits that the gate electrode being 90 nm is not found within Hisao. Yet the Office Action contends, ***without providing any evidentiary support,*** that a gate electrode of 90 nm would have been obvious nonetheless.

In response to this contention, this unsupported assertion amounts to nothing more than conclusions that are personal in nature. The teachings, suggestions or incentives supporting the obviousness-type rejection must be clear and particular. Broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

The Office Action relies upon hindsight for the features missing within Hisao. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. The references themselves must provide some teaching whereby the applicant's combination would have been obvious" (citations omitted). *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). See also *In re Dembiczak*, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999)(rejection based upon hindsight is reversed).

As a rule, "assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

In addition, this assertion amounts to nothing more than an "obvious-to-try" situation. Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990). Moreover, "an invention is 'obvious to try' where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful." *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, the Office Action fails to set forth a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious to try" is not the standard under §103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

Alternatively, another way for a patent applicant to rebut a *prima facie* case of obviousness is to make a showing of "unexpected results," i.e., to show that the claimed invention exhibits some superior property or advantage that a person of ordinary skill in the relevant art would have found surprising or unexpected. *In re Geisler*, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997).

"All evidence of nonobviousness must be considered when assessing patentability." *Richardson-Vicks Inc. v. The Upjohn Co.*, 44 USPQ2d 1181, 1186 (Fed. Cir. 1997).

"Consistent with the rule that all evidence of nonobviousness must be considered when assessing patentability, the PTO must consider comparative data in the specification in

determining whether the claimed invention provides unexpected results." *In re Soni*, 34 USPQ2d 1684, 1687 (Fed. Cir. 1995). See also, *In re Wright*, 6 USPQ2d 1959, 1962 (Fed. Cir. 1988).

In this regard figure 3 of the above-identified application is a graph showing the relation between a film thickness of gate electrodes and a process margin, whereas figure 4 of the above-identified application is a graph showing the relation between a film thickness of the gate electrodes and a quantity of pinholes.

"When an applicant seeks to overcome a prima facie case of obviousness by showing improved performance in a range that is within or overlaps with a range disclosed in the prior art, the applicant must 'show that the [claimed] range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.'" *In re Geisler*, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997).

By making the thickness of the gate electrodes 5 to be less than 100 nm, thermal capacity can be reduced and the difference in thermal condition on the gate electrodes 5 and the insulating substrate 1 is made small, thereby trying to enlarge a process margin occurred by the laser anneal treatment (specification at page 9, line 31 to page 10, line 4). It is also clear from the graph of figure 3 that the film thickness of the gate electrodes is required to be set to less than 100 nm (specification at page 12, lines 14-15). Moreover, figure 4 shows that by making the thickness of the gate electrodes to be less than 100 nm, emergence of the pinholes may almost completely be prevented (specification at page 12, lines 22-23).

If the thickness of the gate insulating film 4 located between the gate electrodes 5 and the semiconductor thin film 2 is too thin, an effect of reducing the thickness of the gate electrodes 5 is offset (specification at page 10, lines 4-7). Therefore, the thickness of the gate insulating film 4 is made to become greater than the thickness of the gate electrodes 5 (specification at page 10, lines 7-9). For instance, when the thickness of the gate electrodes 5 is 90 nm, the thickness of the gate insulating film is made to be 110 nm (specification at page 10, lines 9-11).

"An applicant relying on comparative tests to rebut a prima facie case of obviousness must compare his claimed invention to the closest prior art." *In re De Blauwe*, 222 USPQ 191, 196 (Fed. Cir. 1984).

The Office Action provides Hisao as the closest cited prior art. Yet, the Office Action admits that the gate electrode being 90 nm is not found within Hisao.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: July 7, 2004

Respectfully submitted,

By _____
Ronald P. Kananen
Registration No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750
Attorney for Applicant

APPENDIX A

1. A thin film semiconductor device comprising:

an insulating substrate; and

a thin film transistor formed on said insulating substrate, wherein

said thin film transistor is formed in a bottom gate structure having gate electrode, a gate insulating film, and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

2. The thin film semiconductor device according to Claim 1, wherein

said gate insulating film has a thickness thicker than the thickness of said gate electrode.

3. The thin film semiconductor device according to Claim 1, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

4. The thin film semiconductor device according to Claim 1, wherein

said gate electrode has a multi-layered structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

5. A display device comprising:

an insulating substrate;

pixels arranged in a matrix form; and

thin film transistors for driving said respective pixels, wherein said pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode, a gate insulating film and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100 nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

6. The display device according to Claim 5, wherein

said gate insulating film has a film thickness thicker than the thickness of the gate electrode.

7. The display device according to Claim 5, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

8. The display device according to Claim 5, wherein

said gate electrode has a multi-layer structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

13. The thin film semiconductor device according to Claim 1, wherein the thickness of the gate insulating film is greater than 100 nm.

14. The thin film semiconductor device according to Claim 13, wherein the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

15. The display device according to Claim 5, wherein the thickness of the gate insulating film is greater than 100 nm.

16. The display device according to Claim 15, wherein the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.